APPLICATION NOTE

How to Accurately Test and Characterize the Gate Charge (Qg) of SiC Devices

Correctly and efficiently use dynamic / static parameter analyzer to measure Qg

KEYSIGHT

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Introduction

Gate charge (Qg) is a critical parameter for describing the switching characteristics of power devices (Power MOSFETs/IGBTs) controlled by gate voltage. It refers to the amount of gate charge required for the gate voltage to rise from a certain off voltage (e.g., 0V) to the fully on voltage (e.g., 15 V). The magnitude of gate charge directly impacts the switching performance of power devices. The larger the gate charge, the longer the capacitor charging time needed to turn on the MOSFET, leading to increased switching losses and affects switching speed and efficiency. Therefore, a smaller gate charge facilitates high-speed switching and reduces switching losses. Furthermore, gate charge is also a key parameter in designing gate driver circuits.

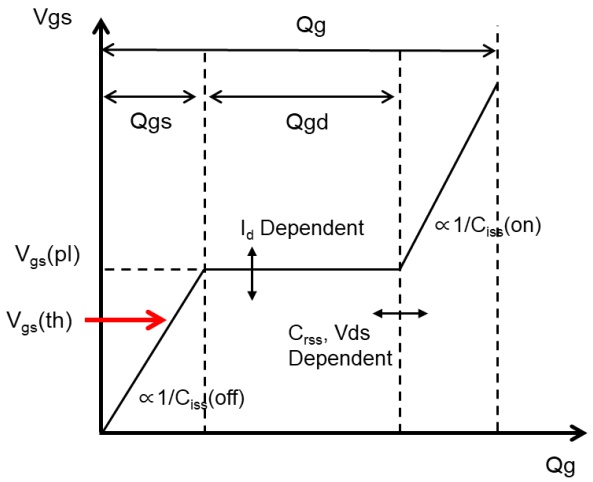


Figure 1. Typical Gate Charge Curve

Gate charge specifications are typically found in the dynamic characteristics tables and characteristic graphs in datasheets, showing the relationship between gate-source voltage and total gate charge. A typical curve is illustrated in Figure 1. The entire process can be divided into the following stages:

1. **Initial Stage:** When the turn-on pulse is applied to the gate and source, the input capacitance Ciss begins charging, and the gate voltage rises linearly.
2. **Threshold Voltage Stage:** When the gate voltage reaches the threshold voltage Vth, current starts flowing through the drain, but the drain-source voltage remains unchanged.
3. **Miller Plateau Stage:** The gate voltage continues to rise until reaching the Miller plateau voltage Vgs(pl), during which the drain current reaches its maximum value, and the drain-source voltage starts to drop.
4. **Steady Stage:** After the Miller plateau ends, the drain current remains at its maximum value, but the drain-source voltage continues to drop until it stabilizes at Vds=Ids(max)×Rds(on).

The gate charge curve helps illustrate the state changes and the variations of current and voltage during the switching process of power devices. By analyzing the gate charge curve, it is possible to better design drive circuits, optimize switching performance, and reduce switching losses.

Qg Measurement with Static Parameter Test Instrument

The traditional gate charge test is completed with static parameter instrument, and then the Qg curve is extracted through algorithm fitting. The following section will introduce how to test Qg with a static parameter test system.

Qg Testing Process with Static Parameter Test Instrument

The testing of gate charge (Qg) typically requires a power source capable of providing a seamless transition from high voltage to high current output. Additionally, the instrument must feature high-precision current and voltage measurement capabilities to ensure accurate results. For standard static parameter test instrument for power devices, high voltage and high current outputs are generally provided by separate power modules.

- **High-voltage modules** are often used for breakdown parameter testing (e.g., BVdss) and do not require significant current output.
- **High-current modules**, on the other hand, are used for testing output characteristics and transfer characteristics, which do not demand high voltage output.

This separation makes it challenging for a single power source to meet the rapid transition requirements from high voltage to high current in Qg testing between the drain and source. Static parameter testing instrument overcomes this limitation by utilizing high-voltage and high-current modules to perform separate tests. The data from these tests are then fitted together by the two-step gate charge measurement method producing a comprehensive Qg result for both high-voltage and high-current conditions. The two-step fitting process is shown in Figure 2.

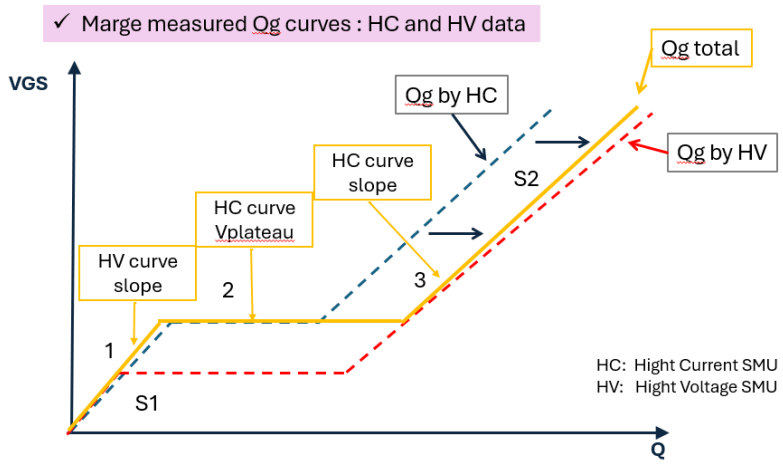


Figure 2. Two-Step Gate Charge Measurement Method

Step 1: Low Voltage/High Current Testing

Using the high-current module, conduct Qg testing with low voltage and high current (as per test conditions). The gate is driven using a constant current source mode that is easy to achieve the integral charge, and the results are shown as the Qg by HC curve in the figure.

Step 2: High Voltage/Low Current Testing

Use the high-voltage module to perform Qg testing with high voltage and low current (as per test conditions). The results are shown as the Qg by HV curve in the figure.

Finally, these two curves are fitted to produce a Qg result that satisfies both high-voltage and high-current testing conditions, represented by the Qg total curve in the figure.

Fitting Process

1. **Extend Segment S1**

   Extend the high-voltage test's Segment S1 upward to the plateau voltage of the high-current test. (Segment S1 correlates with Cgs during Vd(off), and the plateau voltage Vgs(pl) is determined by Id(on).)

2. **Extend the Plateau**

   Extend the plateau until it intersects with Segment S2 from the high-voltage test. (The platform's length is consistent with that of the high-voltage test.)

3. **Extend Segment S2**

   Using the slope of the high-current test results, extend Segment S2 upward. (Segment S2's slope is determined by Ciss during Id(on).)

This process ensures an total Qg measurement that captures both high-voltage and high-current characteristics.

Testing Process Using Keysight Static Parameter Test Instruments

Keysight Technologies offers two versatile static parameter testing instruments for power components: the **B1505A** and the **B1506A Power Device Analyzer**.

1. B1505A
    - Primarily designed for **R&D professionals**.
    - Capable of outputting voltages up to **10 kV**.
    - Supports a wide range of on-wafer parameter testing, including **IV**, **CV**, and **Qg** measurements.

2. B1506A
    - Geared towards **end-users of power devices.**
    - Specifically tailored to verify various datasheet parameters of power devices.
    - Optimized for the **efficient testing of packaged devices.**

These instruments provide comprehensive functionality for precise and reliable static parameter measurements, catering to different stages of power device development and application.

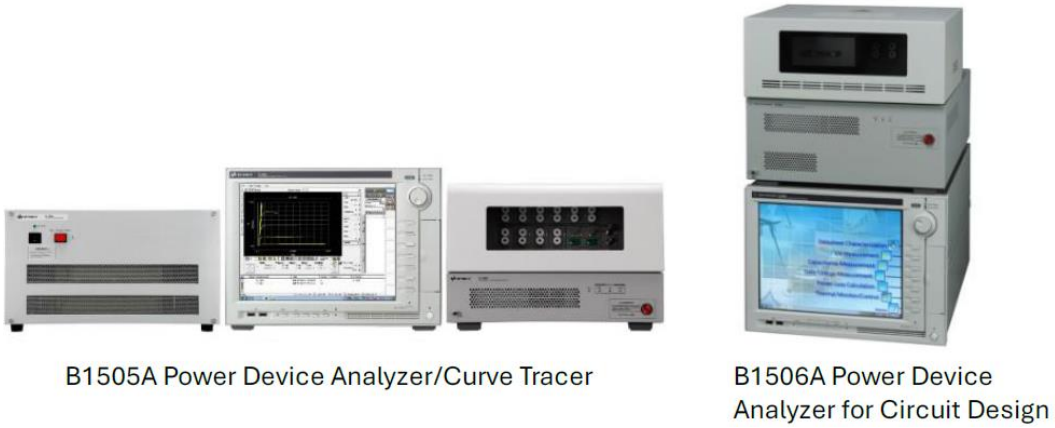


Figure 3. B1505A and B1506A power device analyzer

The following table lists the B1505A and B1506A features and functions.

	B1505A	B1506A
Flexibility	Configurable	Fixed Configuration
Output Range	10 kV / 1500 A	3 kV / 1500 A
Coverage	From small to large devices using a single instrument	500 A / 1500 A versions cannot be used for small sized device (I < 10 A)
Ease of Use	• Requires device knowledge to connect up DUTs • Supported only by EasyEXPERT group+ SW – Requires measurement expertise to get good data	• Automated and simplified DUT connections • Intuitive software (Datasheet Mode of ETN) • Automated switching
IV	• 10 kV /1500 A wide coverage • Can cover 20 A and 1500 A by single mainframe • Sub pA level precision leakage current measurement • Multi-channel measurement (ex. Sense emitter current meas.) • Package and on-wafer • Multiple HVSMU support (up to 5) • Need to wiring manually even for packaged device	• Max.3 kV / 1500 A • For Id < 10 A, 20 A model is required. • For Id > 20 A, 500 A or 1500 A model are required • Sub nA level leakage current • 3 terminal + 1 bias • Package only • Single HVSMU
Qg	• Can cover 20 A and 1500 A by single mainframe • Need to switch HC and HV Qg manually (excluding 20 A on-wafer Qg) • On-wafer Qg is supported	• For Id < 10 A, 20 A model is required • For Id > 20 A, 500 A or 1500 A model are required • Can switch HC Qg and Hv Qg automatically
CV	• IV and CV switching requires manual connection change • On-wafer CV support	• Automated IV and CV switching • Only supports CV on packaged devices
Thermal Test	• IV and CV has to be switched manually by changing the wiring • Need different enclosure for Thermostream and thermal plate	• IV / CV automatic switch • IV / CV under temperature test • Thermal test does not require extra test enclosure

In the Qg testing process, the B1505A and B1506A are also used in conjunction with the HVSMU (High Voltage Source Measure Unit) and UHCU (Ultra High Current Unit) or HCSMU (High Current Source Measure Unit) for step-by-step testing.

High-Voltage Qg Testing with HVSMU

The high-voltage testing process with the HVSMU is relatively simple, as shown in Figure 4. The HVSMU output is set to the required high voltage for the test conditions. When the power device is turned on, the HVSMU will output the maximum current of 12 mA. Figure 5 shows the Qg test curve for a power device under 400 V high voltage conditions.

The gate drive current Ig is a crucial setting. If Ig is set too small, there will not be enough charge to turn on the power device, leading to inaccurate Qg measurement. Specific calculations for Ig can be found in the referenced application note [1].Figure 6 illustrates the switching process of the voltage and current waveforms during the Qg test, as well as the rising process of gate voltage.

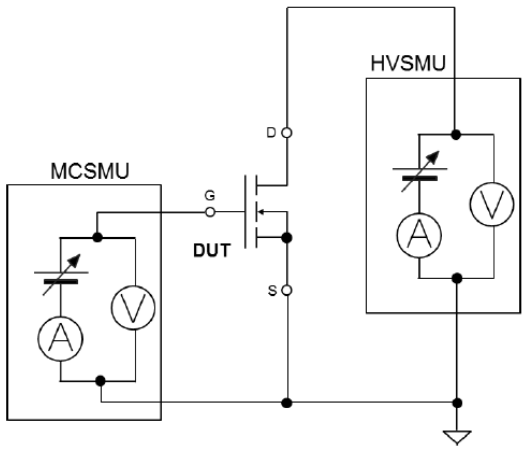


Figure 4. HVSMU Qg measurement scheme

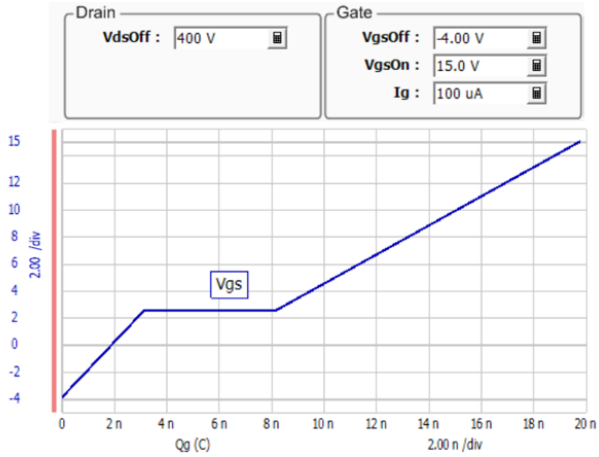


Figure 5. HVSMU Qg measurement curve

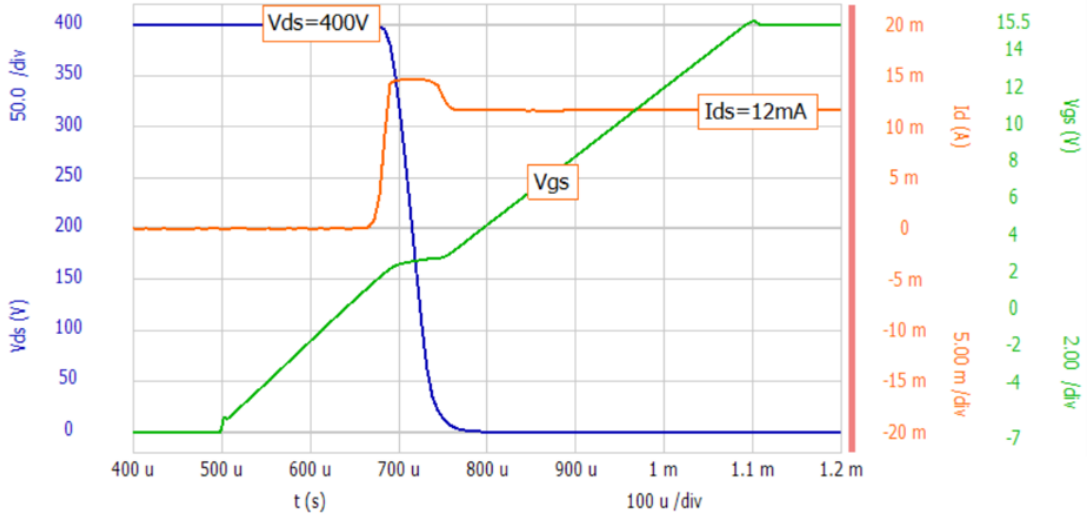


Figure 6. The switching waveforms of HVSMU Qg measurement

[1] https://www.keysight.com/us/en/assets/3124-1556/application-notes/Static-and-Dynamic-Gate-Charge-Measurement.pdf?courseId=98

High Current Qg Testing with UHCU

There are two Qg testing methods for high-current conditions:

- Current load method
- Resistive load method

The process is relatively complex, as shown in Figure 7.

Current Load Method

The output current of the UHCU is set to the required high-current value for the test conditions, and the voltage is typically set to the default maximum output voltage of 60 V.

To ensure that the current during the Qg test remains stable at the set value, the best approach is to use another power device as a current load, connected in series with the device under test (DUT). To maintain a stable current output from the UHCU during the DUT's turn-on, the current load needs to be controlled through the gate voltage to operate in the constant current region (as shown in Figure 8). This method ensures that the current is kept constant during the DUT's turn-on process.

It is essential to select the current load carefully to ensure that its safe operating range can accommodate the current conditions required for the Qg test. Figure 9 shows the voltage and current waveform switching process using the current load, illustrating how the current is maintained stable as the DUT is turned on. This method ensures high accuracy in measuring Qg under high current conditions by utilizing a current load and controlling the current flow through the DUT effectively.

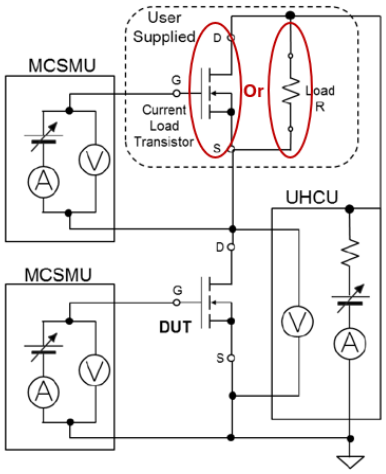


Figure 7. High current Qg measurement scheme

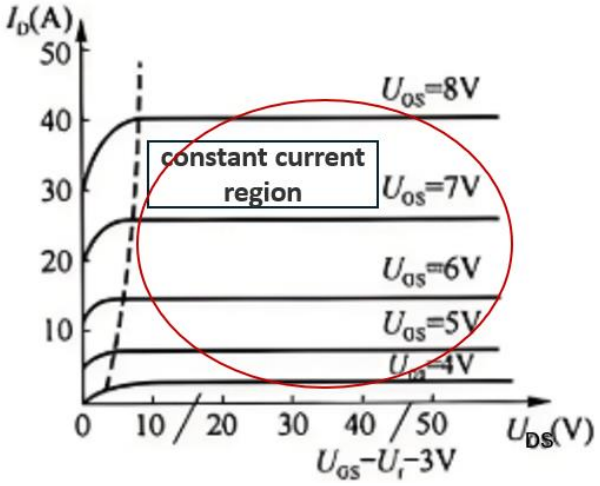


Figure 8. The constant current region of a power MOSFET

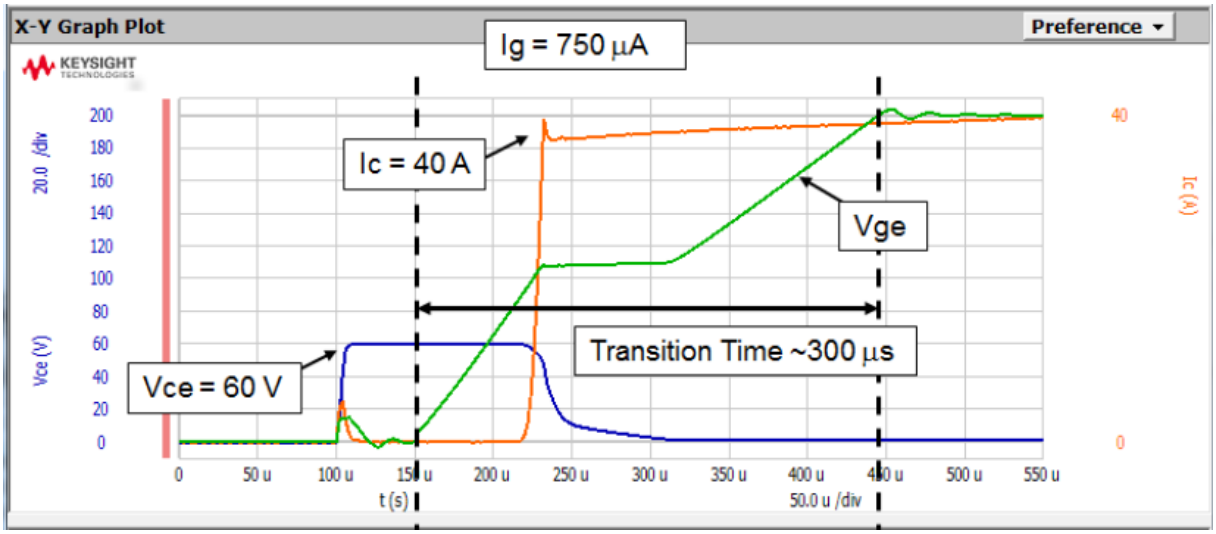


Figure 9. A typical voltage and current waveform switching process using the current load

Resistive Load Method

For power module Qg testing, since the current can be very high—up to thousand amperes—it is often difficult to find a suitable current load. Therefore, the resistive load method is typically used. The principle is shown in Figure 7, where a small resistor is used to replace the current load and is connected in series with the device under test (DUT).

During the test, the UHCU automatically adjusts the output voltage to achieve the output current values during the DUT's turn-on. It is important to ensure that the selected series resistor, combined with the internal resistance of the UHCU, does not cause the current output capability of the UHCU to fall below the set current value.

Figure 10 shows the Qg test waveform for a power module (IGBT) under a current of 1.47 kA. This method may experience variations in Rce during the DUT's turn-on process, which prevents the current output from stabilizing quickly (compared to the current load method). This can lead to a gradient voltage plateau, as shown in Figure 11 with the Qg test curve.

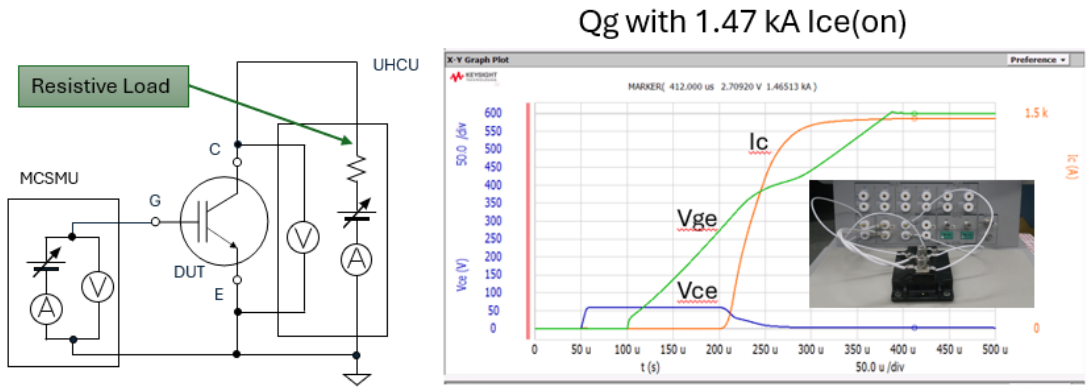


Figure 10. Power module resistive load connection scheme and voltage and current switching waveform

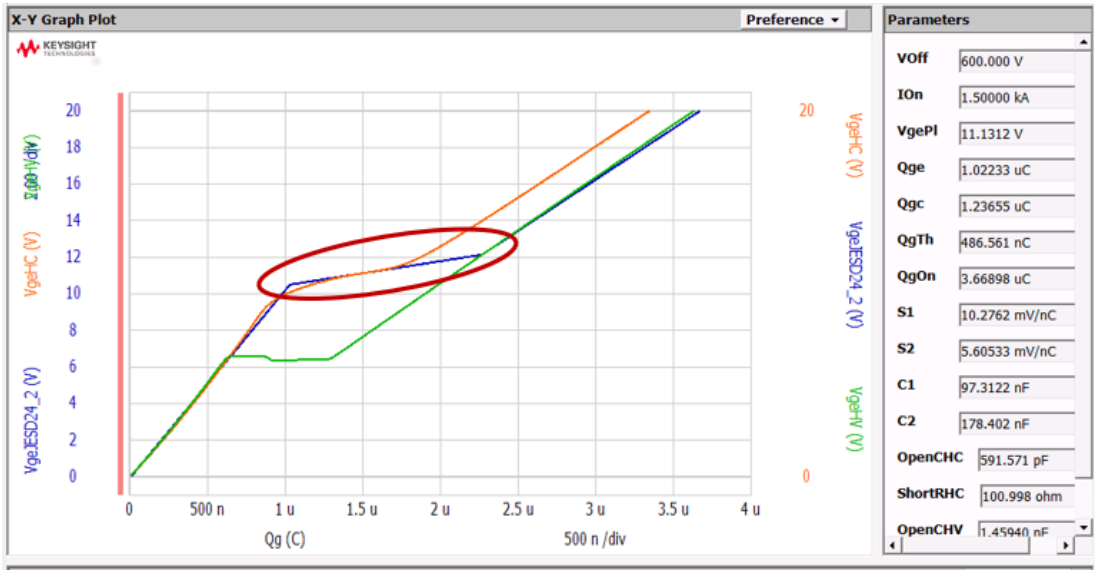


Figure 11. Power module Qg measurement curve

Silicon Carbide (SiC) Devices Qg Measurement

Due to the DIBL (Drain-Induced Barrier Lowering) effect, the output characteristics of SiC devices are different from Silicon devices. Under the same Vgs conditions, the saturation current of the SiC device increases as Vds rises, as shown in Figure 12.

This phenomenon causes the plateau voltage to become Non-level, resulting in a noticeable slope in the plateau voltage during high-current Qg testing. In contrast, the plateau voltage for traditional silicon-based devices remains relatively flat, as shown in Figure 13.

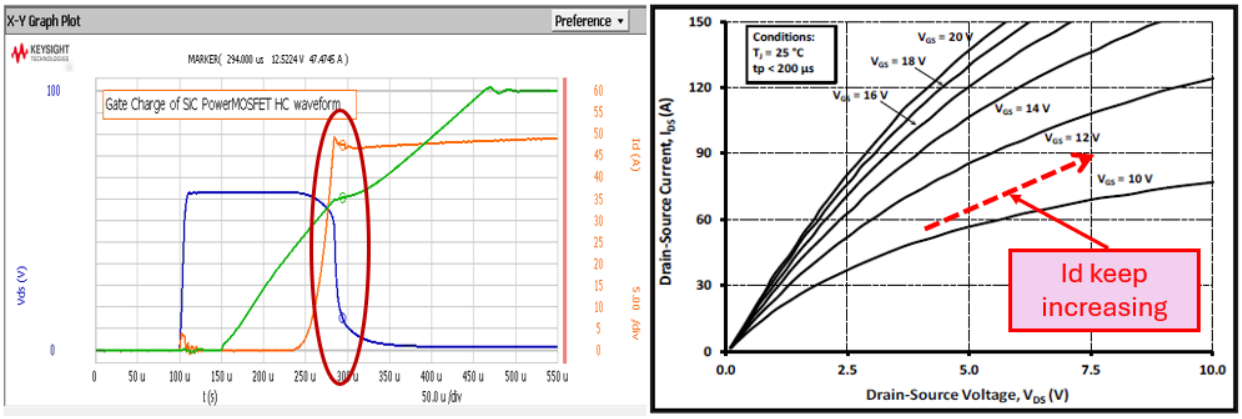


Figure 12. The correspondence between the turn-on process and the output curve of SiC MOSFET

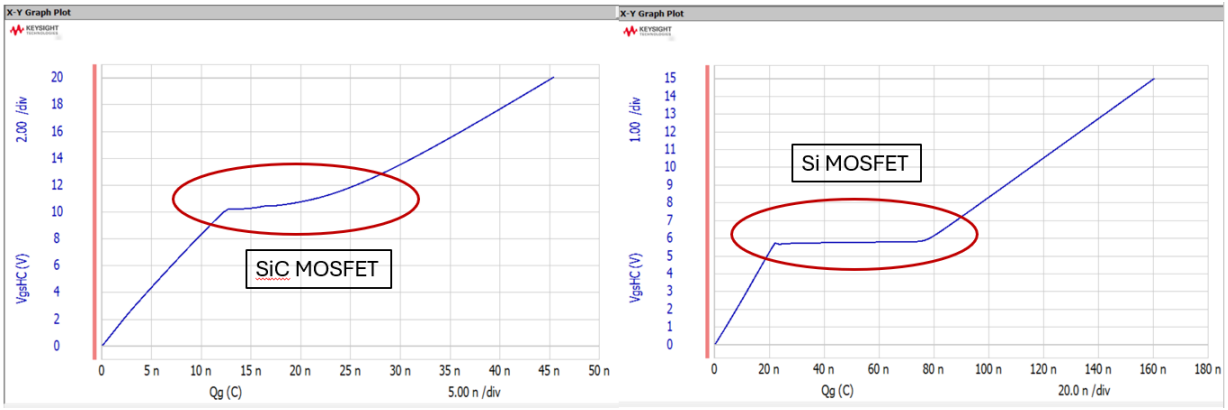


Figure 13. SiC and Si MOSFET high current Qg test contrast

At the same time, for some SiC MOSFETs in our experiments, we observed that during the high-current testing process, the current experiences discontinuous changes in the initial turn-on phase, and the gate voltage fluctuates accordingly. If these fluctuations are significant, they can even lead to oscillations, which may result in misjudgment of the initial slope and Miller plateau when generating the Qg curve. The process is illustrated in Figure 14.

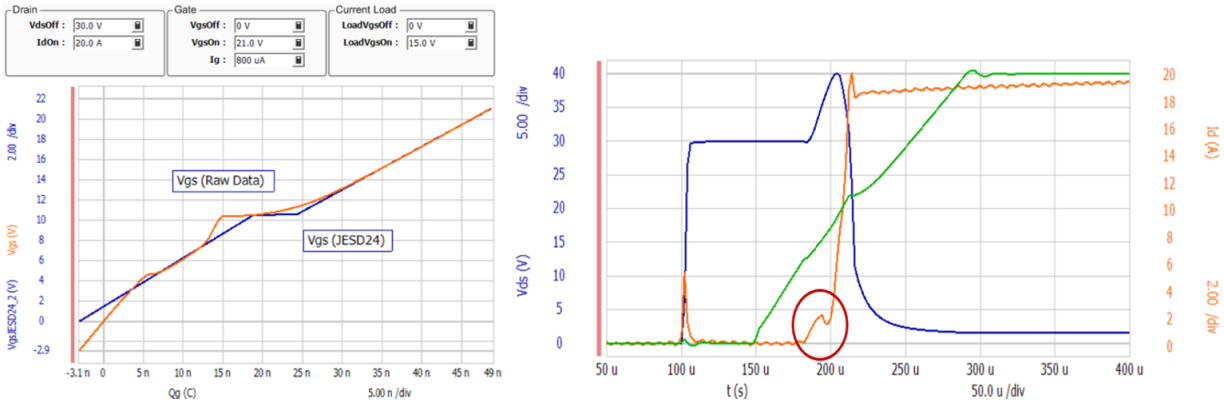


Figure 14. The Abnormal in some SiC device high current Qg measurement

To reduce these abnormal fluctuations, the Vdsoff voltage during high-current testing can be appropriately adjusted. For the B1505A, this adjustment needs to be made in the high-current Qg application test program, while for the B1506A, it can be set in the High Current Setup.

Based on practical test comparisons, appropriately lowering the Vdsoff voltage can effectively reduce the fluctuations in Ids during the initial turn-on phase, allowing the curve to be generated normally. This process is illustrated in Figure 15.

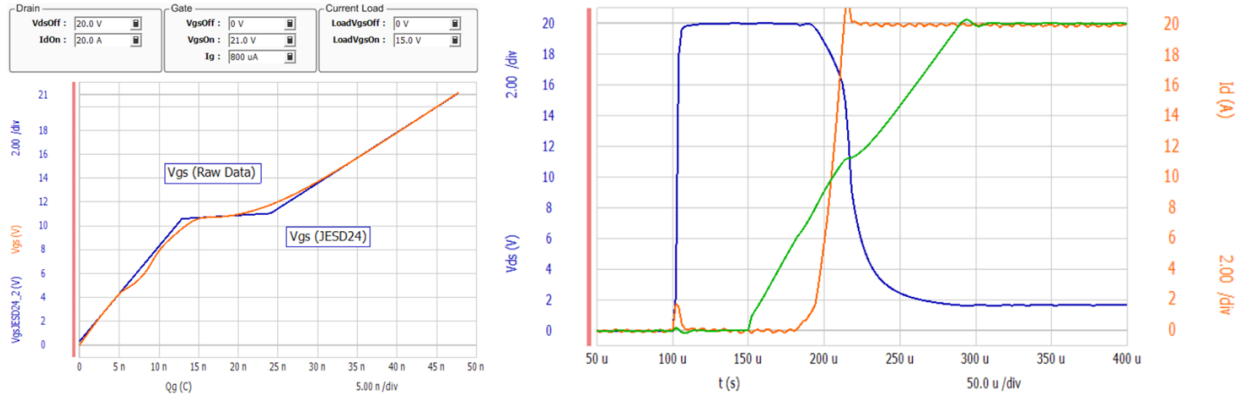


Figure 15. Lowering Vdsoff in high current Qg measurement to reduce the fluctuation

Qg Measurement Tips Using Static Measurement System

1. Selecting a suitable device as the current load can not only provide a constant current but also withstand the voltage and current of the corresponding magnitude to ensure that the test can proceed normally.
2. Set a sufficiently large gate drive current Ig according to the calculation.
3. Appropriately reduce the Vdsoff setting during high current Qg test process.

Qg Measurement with Dynamic Parameter Test Instrument

Another method to measure gate charge is to use a dynamic parameter tester. The semiconductor dynamic parameter analyzer, also known as a double pulse tester, is an essential instrument for testing the dynamic parameters of semiconductor power devices.

Keysight Technologies offers two dynamic test analyzers, PD1500A and PD1550A, as shown in the Figure 16.

PD1500A, primarily designed for measuring Si, SiC, and GaN discrete devices, has measurement capabilities of Vds / Vce up to 1200 V and Ids / Ice up to 200 A. It can measure switching parameters, reverse recovery, Qg, dynamic on-resistance and other parameters. PD1550A, designed for higher measurement capabilities, in addition to testing discrete power devices, it can also measure power modules. It has measurement capabilities of Vds / Vce up to 1500 V, Ids / Ice up to 3000 A, and it can simultaneously measure both upper and lower arms of a bridge, also includes short-circuit testing capability. These analyzers are essential tools for accurately testing the dynamic characteristics of semiconductor power devices under high voltage and current conditions.

PD1500A

PD1550A

Figure 16. Keysight Technologies Dynamic Parameter Measurement System Series

The main features of PD1500A and PD1550A are shown in the following table

	PD1500A	PD1550A
Functionality	• Turn-On / Turn-Off Characteristics • Switching Characteristics • Reverse Recovery • Gate Charge • Derived Output Characteristics (IdVg, IdVd)	• Turn-On / Turn-Off Characteristics • Switching Characteristics • Reverse Recovery • Gate Charge • Derived Output Characteristics (IdVg, IdVd) • Short Circuit Test
Output Range	1200 V / 200 A	1500 V / 3000 A
Coverage	• Power Discretes: Si, SiC, GaN	• Power Discretes • Power Modules
General	• Sample Rate :16 GSa/s • Sampling Accuracy: 8 ppb + 75 ppb / year • Deskew Accuracy: 200 ps (typical)	• Sample Rate :16 GSa/s • Sampling Accuracy: 8 ppb + 75 ppb/year • Deskew Accuracy: 200 ps (typical)
Drain/ Collector Channel	• Output Max:1200 V / 200 A • Voltage Programming Resolution:23 mV • Measure Voltage Accuracy: 2% of range • Measure Current Accuracy 4% of range • Voltage Measure Bandwidth:500 MHz • Current Measure Bandwidth: 400 MHz (typical)	• Output Max:1500 V /3000 A • Voltage Programming Resolution:23 mV • Measure Voltage: < 2000 V, accuracy 2% of range • Measure Current:< 5000 A, accuracy 4% of range • Voltage Measure Bandwidth:400 MHz • Current Measure Bandwidth: 200 MHz / 400 MHz (typical)
Gate	• High / Low Level Voltage Output: -28 V to 0 / 0 to +28 V • Voltage Resolution: < 0.1 V (typical) • Typical 1st Pulse Width: 1 to 60 µs • Off-Time between 1st and 2nd Pulse: 25 ns to 25 µs • Pulse Width (2nd Pulse): 200 ns to 10 µs • Voltage Measure Bandwidth:500 MHz • Current Measure Bandwidth: 800 MHz	• High / Low Level Voltage Output: -28 V to 0 / 0 to +28 V • Voltage Resolution: < 0.1 V (typical) • Typical 1st Pulse Width: 1 to 60 µs • Off-Time between 1st and 2nd Pulse: 10 µs to 200 µs • Pulse Width (2nd Pulse): 1 µs to 25 µs • Voltage Measure Bandwidth:200 MHz • Current Measure Bandwidth: 200 MHz

Double Pulse System Measurement Principle

The system uses a half-bridge circuit structure to test the parameters of the DUT such as turn-on, turn-off, and reverse recovery parameters. The lower arm of the half-bridge circuit is the DUT, and the upper arm is the companion device, whose body diode is used for freewheeling. An inductor is used as the inductive load of the DUT. The test process is as follows:

1. **Pre-test Setup**

   Before the test begins, an external power supply Vdd charges a large capacitor bank C to the set voltage. Once charged, the power supply is disconnected, and the capacitor supplies power to the test circuit during the test.

2. **First Pulse**
   Two pulses will be generated during the test. The first pulse is generated by turning on the lower MOSFET (DUT). During this process:

   - The gate-source voltage (Vgs) begins to rise.
   - Once Vgs reaches the threshold voltage, the drain-source voltage (Vds) starts to decrease, and the drain current (Id) begins to increase, as shown in Figure 17.

3. **Turn-off Process**
   Once Id reaches the set current, the lower MOSFET is turned off. The gate voltage (Vgs) decreases first, followed by Vds and Id, which reverse their directions. This phase represents the turn-off process of the MOSFET, which lasts from tens to a few hundred nanoseconds, and the dynamic turn-off parameters of the MOSFET are measured during this period. Simultaneously, the current in the load inductor switches to the freewheeling diode loop of the upper MOSFET, maintaining the set current value, as shown in the middle diagram of Figure 17.

4. **Second Pulse**

   After the lower MOSFET is fully turned off, it is turned on again to start the second pulse. At this point, the current maintained in the freewheeling diode loop of the upper MOSFET is redirected to flow back into the lower MOSFET. This represents the turn-on process under the set Id condition, and the dynamic turn-on parameters of the MOSFET are measured during this phase, as shown in the rightmost diagram of Figure 17.

5. **Final Measurements**

   After the MOSFET is fully turned on, the entire dual-pulse measurement concludes. The system will control the MOSFET to turn off and switch the circuits to discharge the inductor and capacitor. Data collection and measurements are then performed.

6. **Parameter Extraction**

   Based on the measured waveforms and test specifications, various parameters such as Turn-on Delay Time $Td(on)$, Turn-on rise time T_r, etc. These parameters are essential for characterizing the dynamic switching behavior of the device under test.

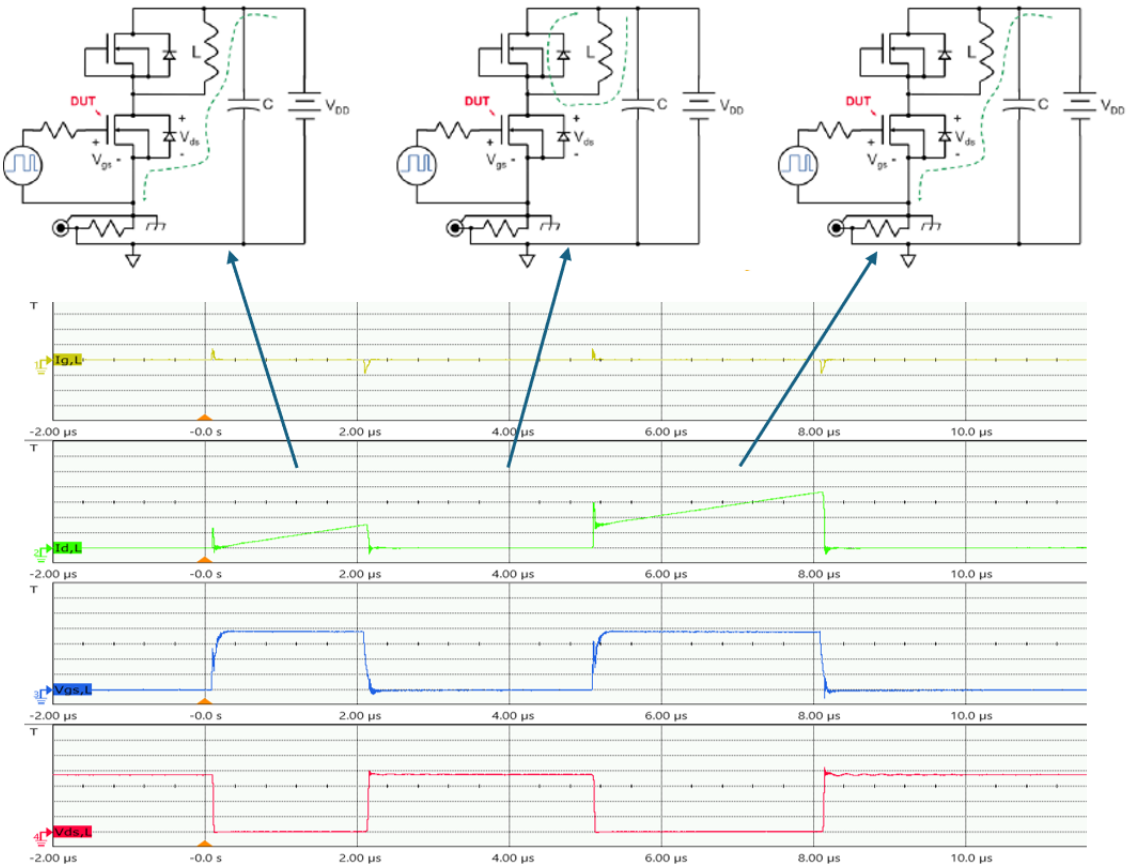


Figure 17. Double pulse test system principal diagram

The above outlines the measurement process for the dual-pulse system. However, it is important to note that the test waveforms are not always as ideal as those shown in the diagram. Since parameters are extracted from the waveforms, the closer the waveforms are to the theoretical ideal, the more accurate and repeatable the measurement results will be.

Nevertheless, many factors influence the accuracy of the waveforms, such as the device's inherent characteristics, stray capacitance from test fixtures, system frequency response, time-domain measurement principles, and so on. In the following sections, we will discuss these factors in detail, as they are crucial for understanding the influence on the measurement accuracy and reliability of the results.

Gate Charge (Qg) Measurement Principle

Using a DPT system to test Qg is not complex. As described by the following formula, the gate charge is the integral of the gate current. We can obtain the Qg-t curve by integrating the Ig-t curve (Curve 1 in Figure 18). Therefore, the Qg-t curve and the Vgs-t curve (Curve 3) must be transformed using an X-Y transformation, which then results in the Qg-Vgs total curve (Curve 4).

$$Q = \int I \times t \, d_t \tag{1}$$

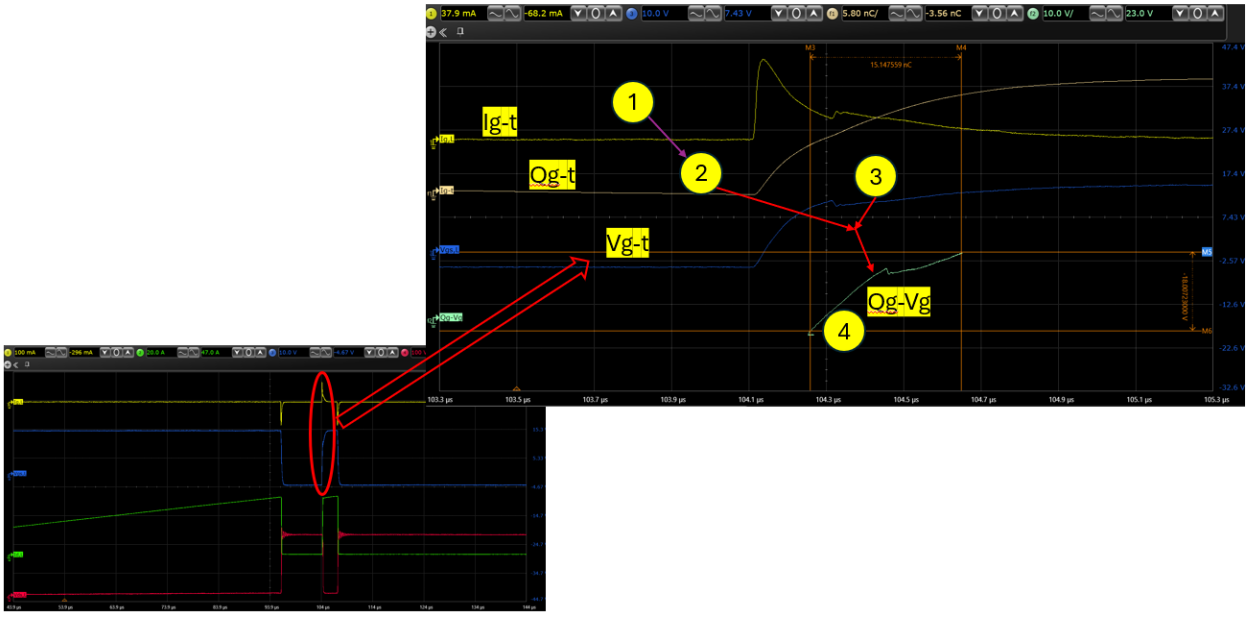


Figure 18. Qg measurement principle

The boundary values for the integration are set according to standards. For example, according to JESE24_2, the entire Qg curve is divided into three segments:

1. **S1:** The turn-off region of the device.
2. **S2:** The turn-on region of the device.
3. **S3:** The Miller plateau region.

Starting from time t0, the integration is performed as follows:

- From t0 to t1, this is the charge associated with Qg_s(th) (threshold gate charge).
- From t0 to t2, this is the total Qg_s (gate charge associated with turn-on).
- From t2 to t3, this is the Qg_d (drain charge).
- From t0 to t4, this gives the total Qg_total (total gate charge).

For the new SiC standard JEP192, the method for determining the integration boundaries differs from that of JESD24-2. This will be discussed in later chapters.

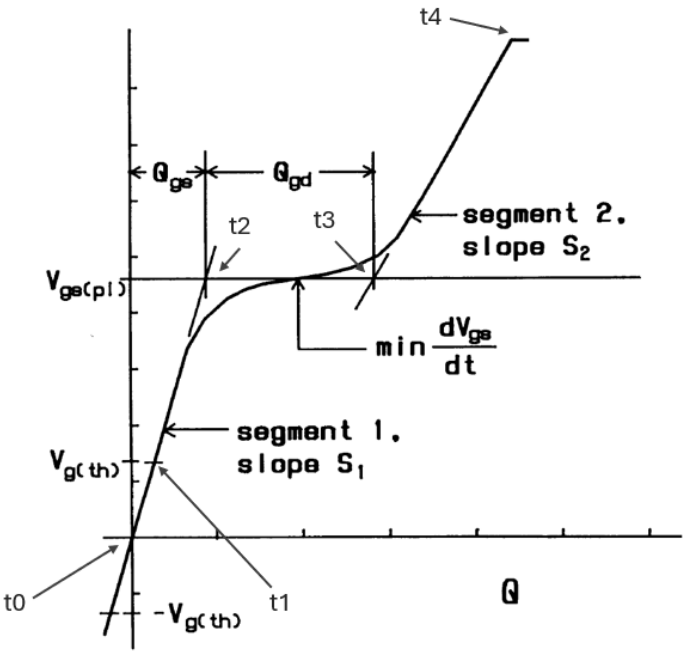


Figure 19. The boundary values of the Qg integration [2]

[2] JESD24-2, “Gate Charge Test Method” (JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, JANUARY 1991 (Reaffirmed: OCTOBER 2002)),page 3

Selection of Gate Resistor (Rg)

The previous sections presented ideal curves, where both the gate current (Igs) and gate-source voltage (Vgs) are relatively smooth. However, in actual measurements, due to the stray inductance present in both the device under test (DUT) and the test fixtures, two main side effects can occur.

- The parasitic capacitance between the device's pins and the stray inductance can cause LC oscillations, leading to waveform instability.
- Rapid changes in current can generate induced electromotive force (EMF), causing unwanted triggering or "spurious turn-on" of the device.

As shown in Figure 20, factors influencing the gate circuit include the stray inductance of the drive circuit (Lg) and the common source inductance (Lss) of the MOSFET's source terminal.

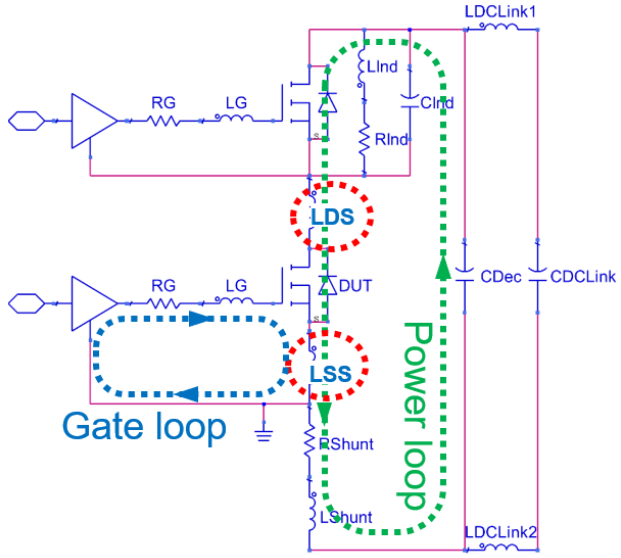


Figure 20. Diagram of Parasitic Components in the Test Circuit

For example, in a fast switching SiC MOSFET device, when the gate resistor (Rg) is set to a standard value for switching tests (e.g., 2.5 Ω), the waveforms of Vgs and Igs are not smooth. As shown in Figure 21, a smaller Rg can easily form an RLC oscillation with stray inductance (Lg) and the MOSFET's gate capacitance (Cgg). Additionally, the rapidly changing current induces a voltage that interferes with the gate loop, causing the Igs and Vgs waveforms to become irregular and unsmooth.

This results in the inability to perform an effective Qg integration, and in the integration plot, the expected Qg-Vgs relationship and the Miller plateau could not be clearly found.

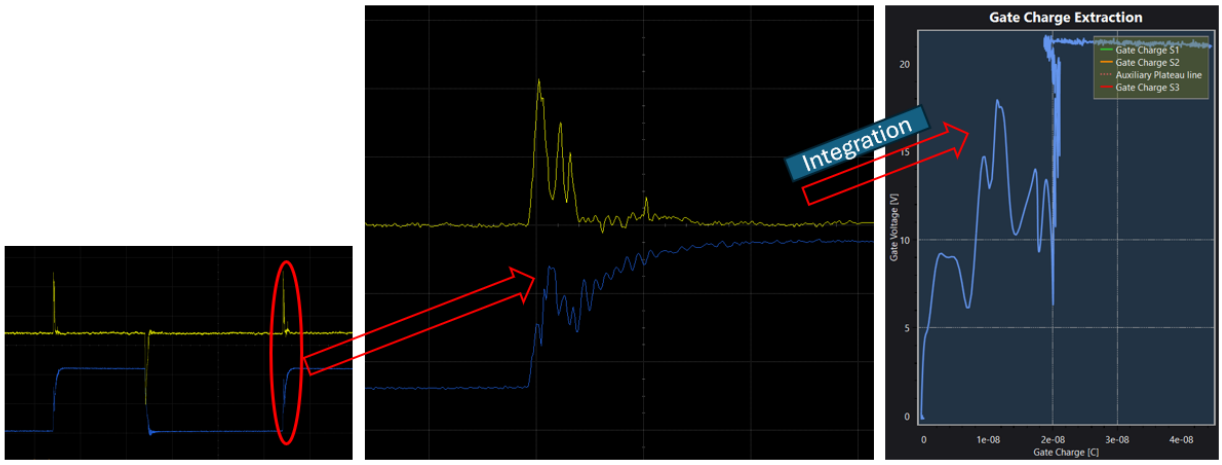


Figure 21. Switching waveform and Qg test results with small Rg

In this case, an effective method is to replace Rg with a larger value. This slows down the turn-on speed of the MOSFET, reducing LC oscillations and minimizing the impact of induced voltage, resulting in smoother curves. It is important to note that since Qg_total is the charging of both Ciss (input capacitance) and Crss (reverse transfer capacitance), slowing down the turn-on speed does not affect the total charge.

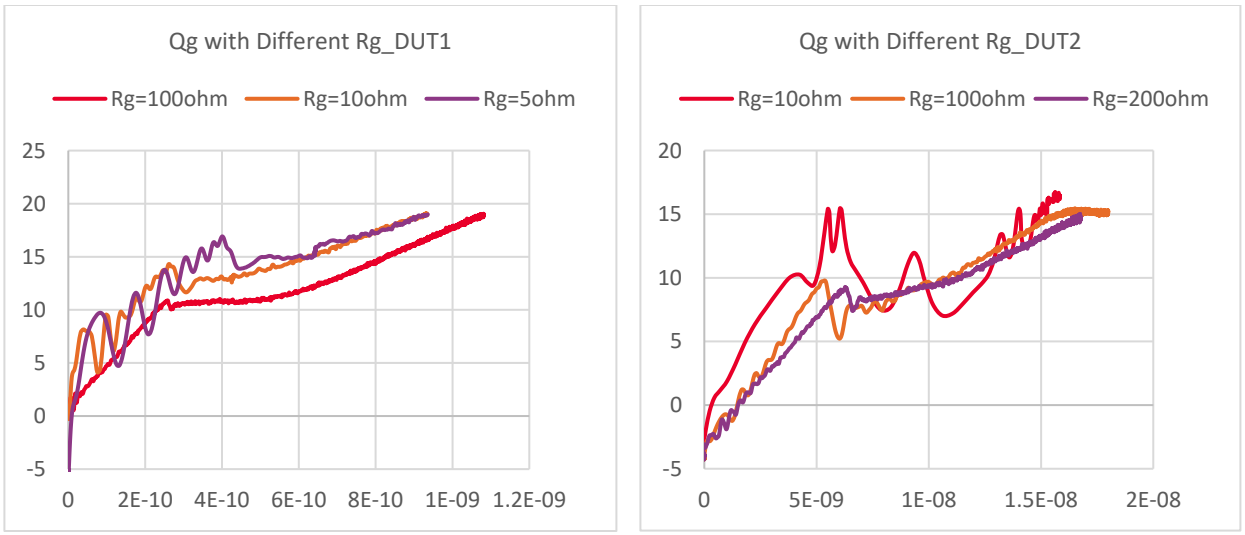


Figure 22. Comparison of Qg Test Results of Different Rg values

As shown in Figure 22, when Rg increases, the Qg curve becomes closer to the ideal shape. This demonstrates that a larger Rg helps to reduce waveform irregularities, resulting in more accurate and reliable Qg measurements, without changing the total gate charge.

In a word, unwanted effects can distort the measurement waveforms, making it crucial to manage the stray inductances carefully. Proper selection of the gate resistor (Rg) helps mitigate these issues by slowing down the switching process, reducing oscillations and unwanted turn-on behavior, and allowing for smoother waveforms.

Constant Current Diode Drive vs. Resistor Drive

In practical applications, gate driving sometimes uses a constant current source instead of a resistor (Rg) for driving the gate, as shown in Figure 23. Theoretically, when using a constant current doide, the gate charging current should be I_const, and when measuring Qg, the relationship Qg(t) = Iconst * t can be used to easily derive the Qg_total curve. This method seems easier than using an high bandwidth oscilloscope probe to measure the current curve, and then integrating it.

However, in practice, establishing a constant current with a constant current diode takes time, meaning that the current is not truly constant at the start of charging. Additionally, as Vgs approaches the setting high voltage, the current from the constant current diode starts to decrease, and thus the current is no longer constant by the end of the process. This leads to errors in the calculation of Qg(t), making it unsuitable to use a constant current diode for gate driving.

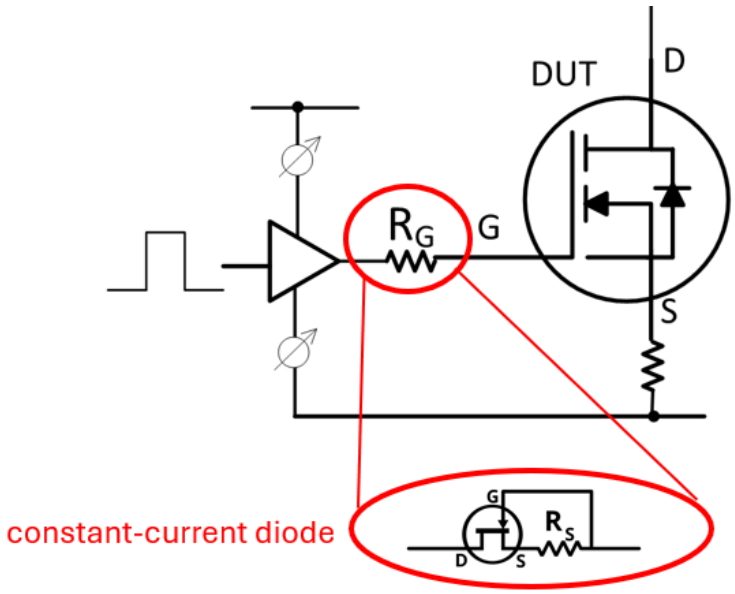


Figure 23. Constant Current Diode as Gate Driver

Optimize Qg Measurement by Setting Appropriate Switching Time, Inductive Load, and Gate Voltage

According to the analysis in the previous chapter, a larger Rg is is beneficial for achieving more ideal results. However, this does not mean that a larger Rg is always better. There are many other factors to consider in a DPT system.

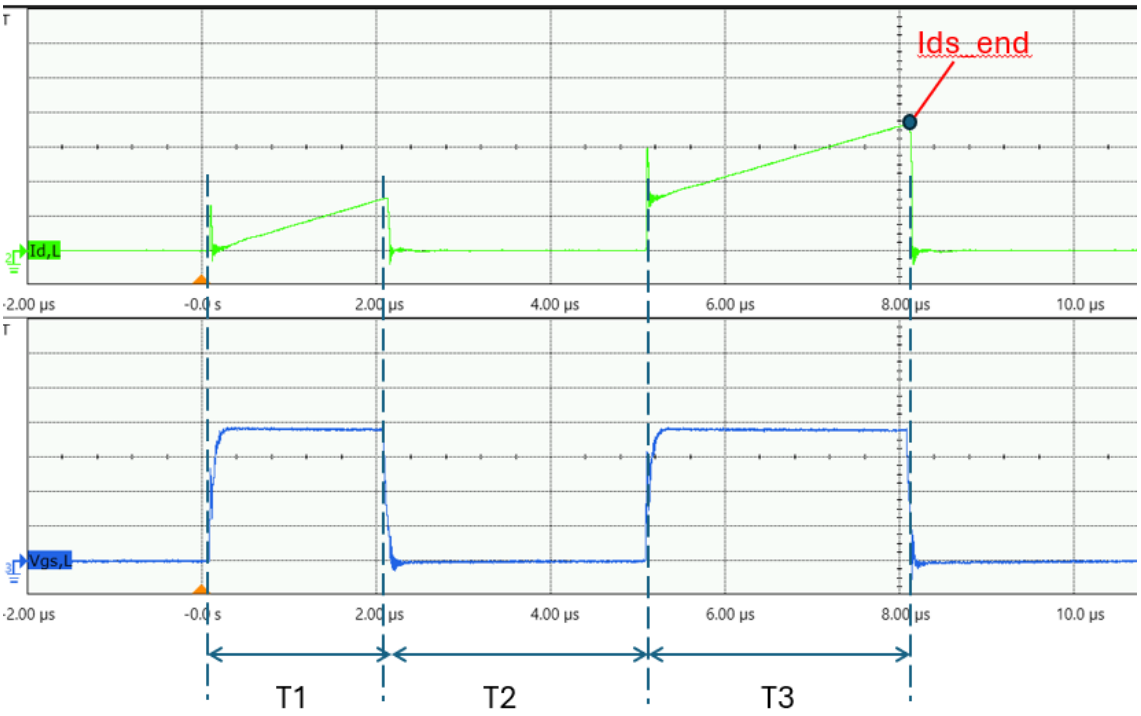


Figure 24. Double Pulse Timing Diagram

First, as shown in Figure 24, there are three typical times intervals for DPT

T1: Inductor charging time

This time cannot be set directly, it is determined by the set Vds value, Ids value and inductor load. The formula is T1 = Ids* L_load / Vds , that is, T1 increases as L_load increases.

T2: Turn Off Time

the gate off time can be set to ensure full shutoff

T3: The second pulse on time

the gate opening time can be set to ensure full opening, Vgs reaches the set value, and Ids enters the linear growth area from the oscillation area at the start time.

Therefore, if Rg increases, , the primary impact is that both gate charging and discharging slow down, and Vgs takes longer to reach the set value. This directly causes T3 to require more time. Without sufficient time for T3, it is impossible to obtain the correct Qg_total.

However, according to the formula below. If T3 becomes longer, the inductance will continue charging during the second pulse, which can cause the final value of Ids_end to exceed the maximum current capability of the device, or the DPT system's maximum allowable measurement current. Additionally, T2 will also need more time to ensure the device is fully turned off.

$$Ids_{end} \approx Id_{set} + Vds \times T3/L_{load} \quad (2)$$

To prevent Ids_end from exceeding the maximum current, a larger inductive load can be selected to reduce the current rise rate. However, this introduces new challenges:

1. The T1 charging time increases, which leads to longer overall measurement and data collection time, increased data volume, and longer data analysis time.
2. The basic principle of DPT is that the capacitor charges the inductance, and as the capacitor discharges, the energy is transferred to the inductor, causing a voltage drop. According to the following formula, increasing L_load will increase the voltage drop across the capacitor. In extreme cases, such as low voltage, high current conditions, it'll fail to meet the test set request.

$$\frac{1}{2}C{V_{ds_{set}}}^2 - \frac{1}{2}C\left(V_{ds_{set}} - \Delta V\right)^2 = \frac{1}{2}L_{load}{I_{ds}}^2 \quad (3)$$

To achieve the most accurate Qg measurement, the test system should offer a variety of Rg boards and various inductors. During Qg testing, try using different resistances such as 50 Ω, 100 Ω, 200 Ω, or even higher. When Igs and Vgs oscillations are sufficiently suppressed, select a larger inductor to prevent Ids_end from exceeding the maximum current. Therefore, for the test system, this is a balanced process.

Also, observe the DPT test waveform for any signs of rapid capacitor energy drop. The more finely tuned the Rg and L_load settings are, the better the chances of finding the optimal test settings. However, it is important to note that the Rg resistor should not use a knob-type adjustable resistor design, as this can degrade the accuracy of Rg and introduce additional stray inductance, which would defeat the purpose. Therefore, for the test system, this is a balance choice.

Keysight 's DPT system PD1500A and PD1550A test fixtures offers a replaceable Rg design and are equipped with an EEPROM to store Rg values, as shown in Figure 25. This ensures low stray inductance in the gate loop, while allowing for the storage and automatic retrieval of calibrated Rg values for easier testing. In addition to the internally provided inductor, an external custom inductor could also be used for optimization.

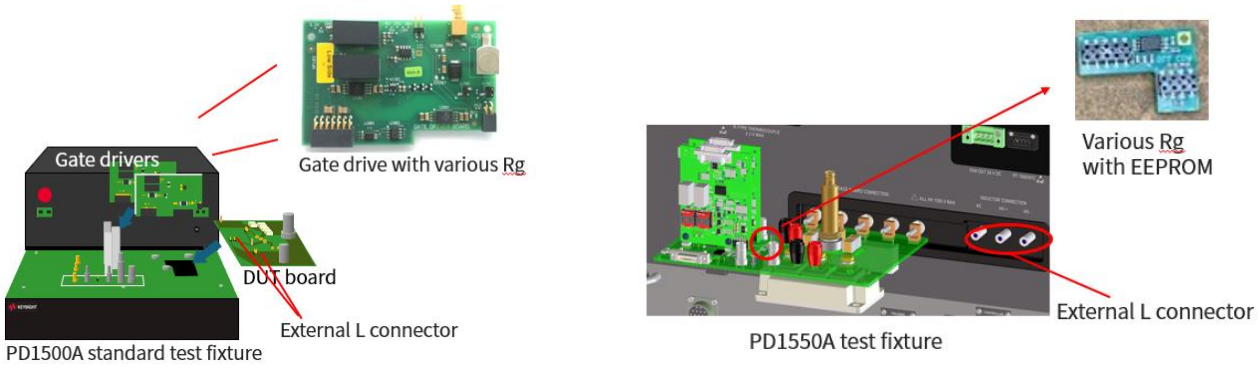


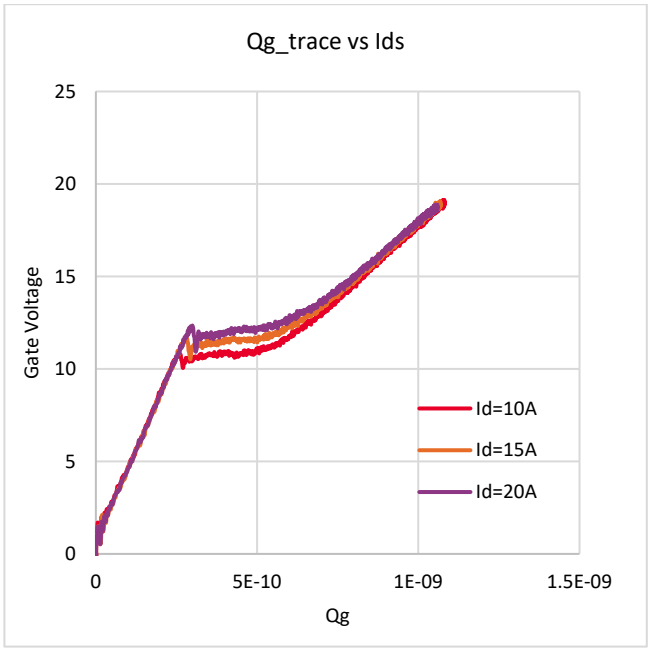
Figure 25. DPT Test Fixtures of Keysight

Impact Of Different Current And Voltage Conditions On Qg Results

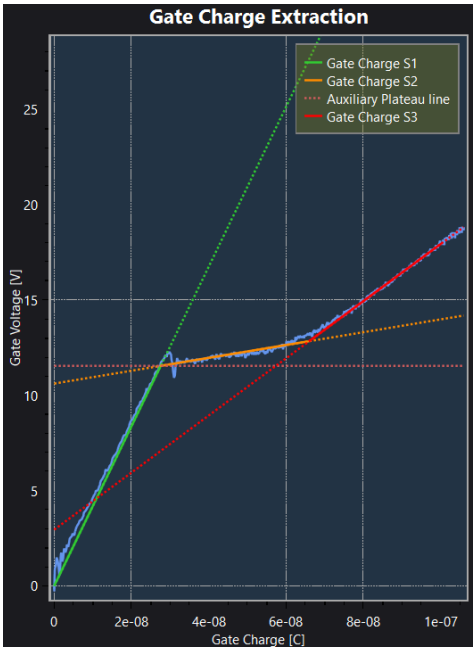
The results of Qg are influenced by different current and voltage conditions, specifically the operating current Vds and Ids.

Effect Of Different Current Conditions

Using the Keysight DTP tester, it is convenient to scan and test Ids, and then compare the results. As shown in Figure 26a, when other conditions remain unchanged, Qg_total increases slightly as Ids increases, though the change is minimal. However, the Miller plateau voltage (Vgs_pl) clearly shifts upward with increasing current, and Qgs_pl also increases with current. This aligns with the principles discussed in the first chapter. Figure 26b shows the Qg fitting line based on the JEP192 standard, and Qgd is basically not affected by changes in Ids.



a. Qg Results with Different Ids



b. Qg Parameter Expansion

Figure 26. Qg Curve vs. Ids Change

The following table lists the Qg expansion parameters difference as Ids change.

Id	Qg (nC)	Qgd (nC)	Qgs_pl (nC)	Vgs_pl (V)
10	101.1	29.56	24.17	10.4
15	100.2	29.72	26.29	11.09
20	99.74	29.78	27.58	11.55

Effect of Different Voltage Conditions on Qg Results

Using the Keysight DPT tester, it is easy to scan Vds and compare the results. Figure 27 shows the measured Qg curve of a SiC module. It is evident that as Vds increases, the turn_on Qg curve(S2) after the Miller plateau(S3) increases significantly with Vds. Figure 27 shows the measured Qg curve for a SiC module. It is evident that as Vds increases, the Qg integration curve after the Miller plateau increases significantly with Vds. Figure 28 directly demonstrates the relationship between the expanded Qg values and voltage. Both Qg_total and Qgd show a linear increase with Vds, which is consistent with the principles of Qg behavior discussed in the first section of this chapter.

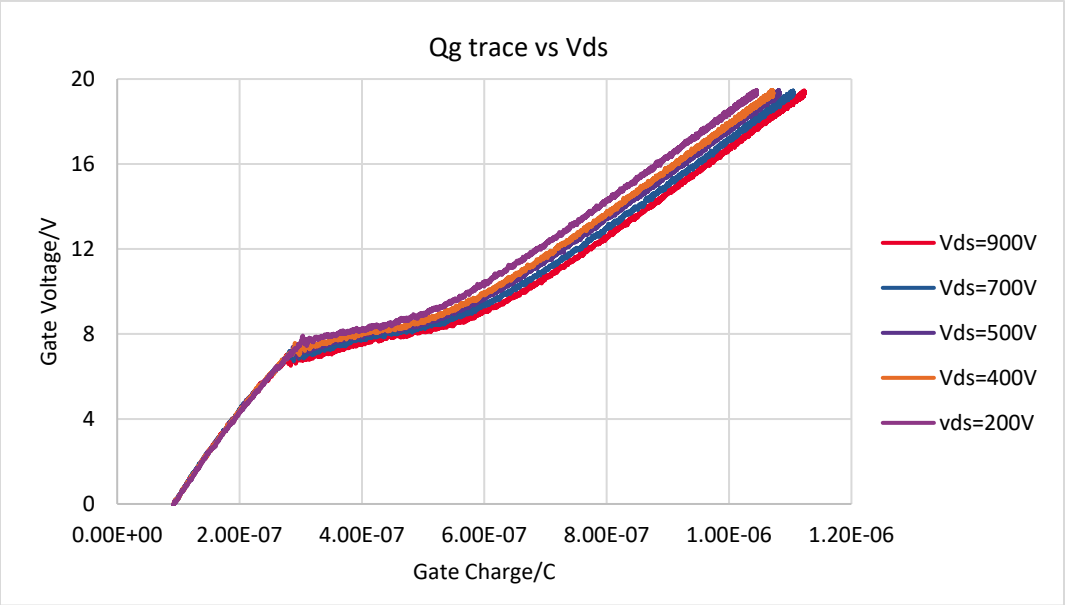


Figure 27. Qg Curve vs. Vds

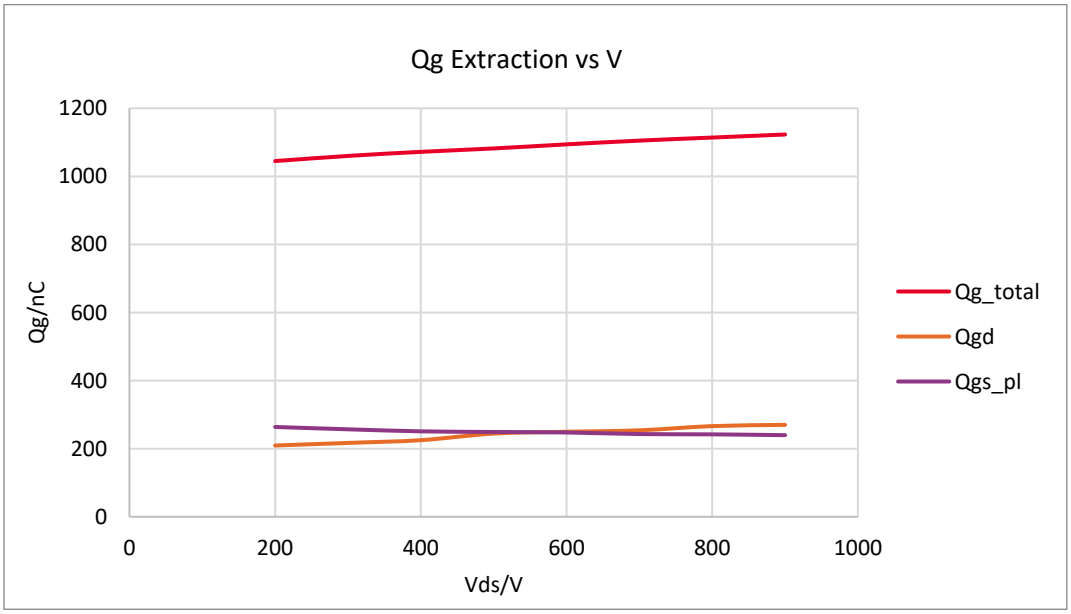


Figure 28. Qg Extraction Parameter vs. Vds

Measuring Qg With Resistive Load

As previously mentioned, when using an inductive load in DPT, parasitic parameters in the circuit and DUT can cause significant waveform oscillations, and the Qg waveform obtained from integration will also exhibit noticeable oscillations. However, this test setup is closer to real-world testing conditions. In some specific scenarios, a resistive load is used instead, and a single-pulse test circuit is applied for dynamic parameter testing. Figure 29 Shows a principal diagram that using DPT for single-pulse test.

In the single pulse testing setup, the load is replaced with a resistor, and there is no need for a diode for freewheeling. Once the device turns on, the current is directly determined by Vds/R_load. After a brief period, the current behaves as a constant current within the pulse. Some legacy SiC devices in the market also used a resistive load for Qg testing as specified in their datasheets. For devices with large parasitic parameters, inductive loads can cause significant oscillations, whereas resistive loads result in much smoother waveforms.

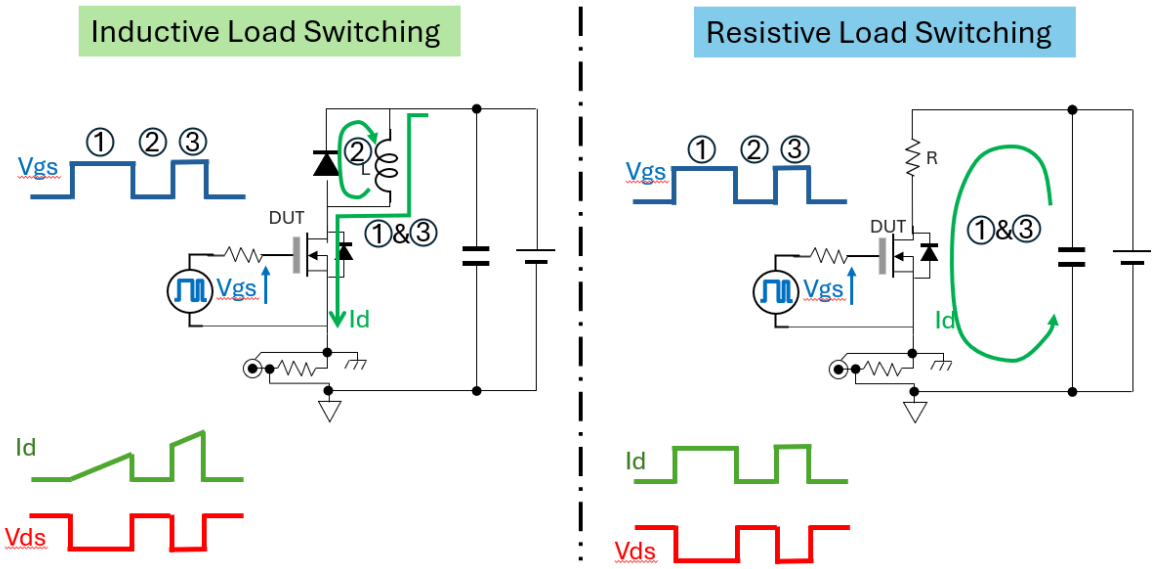


Figure 29. Single pulse test schematic

Keysight's DPT System also supports resistor loads and the expansion of Qg measurements. Figure 30 shows the differences in the Qg curves for a Si IGBT under the same test conditions, using different type of load. It is evident that the inductive load causes noticeable waveform oscillations in the Vgs and Igs waveforms, resulting in significant Qg oscillations as the curve enters the Miller plateau. Even with a larger Rg, the improvement is not significant. In such cases, switching to a resistive load yields a much smoother Qg curve.

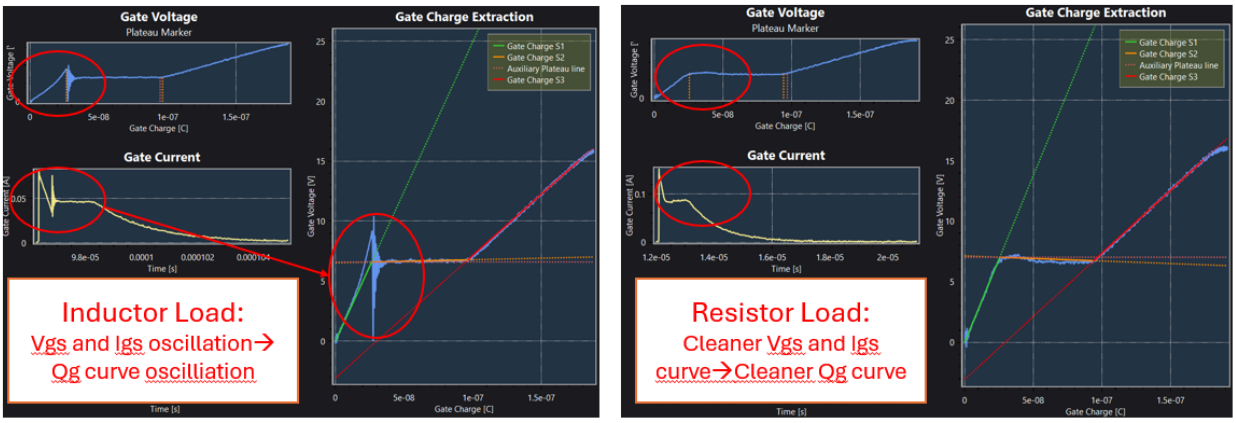


Figure 30. Qg Measured With Inductive or Resistive Loads

Qg Measurement Tips Using DPT Systems

1. **Choose an Adequately Large Rg**
   Select a sufficiently large Rg to slow down the device's turn-on speed, reducing the impact of parasitic elements. This will help achieve smoother curves and better parameter extraction.

2. **Increase T2 and T3 Time After Slowing Down Turn-On**
   When the device turn-on is slower, increase the time for T2 and T3 to ensure that Vgs reaches the set voltage.

3. **Adjust Inductive Load to Ensure Current Limits Are Not Exceeded**
   Increase the inductance value to ensure that the final current measurement does not exceed the device's maximum current capability.

4. **Use Resistive Load for Qg Measurement for Special Cases**
   A resistive load can also be used to measure Qg, especially when the curve exhibits significant oscillations or when the platform charge is large. Resistive loads help smooth out the waveform.

5. **Set a Slightly Higher Vgs Turn-Off Voltage**
   Set the Vgs turn-off voltage slightly higher than the measurement condition to ensure that the actual Vgs during testing reaches the required level.

Understanding The New SiC MOSFET Qg Test Standard JEP192

Due to the unique characteristics of SiC (Silicon Carbide) as a representative of third-generation semiconductors, certain testing methods need to be redefined, as they differ from Si (Silicon) devices. International standard organizations have worked to update or introduce new specifications for SiC. For example, the JEDEC standard association established the JC70.2 SiC New Rules Working Group in 2016, and since 2021, several new guidelines have been released. In January 2023, the JEP192 guidelines were published, titled “Guidelines for Gate Charge (Qg) Test Method for SiC MOSFET" [3], specifically for SiC devices and modules. According to this new standard, SiC devices or modules must be tested following the new guidelines, while Si devices can still be tested according to the old standard (JESD24-2, IEC60747-8).

There are several key differences in the new Guidelines:

1. **Different Test Circuit Design**

   The old standard did not specify a DPT method but only provided basic circuit diagrams, such as Figure 31b and Figure 31c. These diagrams used a current source to drive the gate and measured Vgs voltage, essentially using a static testing method. Additionally, the load type was not specified, and the testing details were insufficient. For example, the current levels during turn-off and turn-on section were significantly different, and no guidance was provided on how to handle this.

   The new JEP192 rules clearly provide two test circuit diagrams. Figure 31a.1 is a double pulse test schematic diagram, which belongs to the newly added dynamic test method. It clarifies that the following tube is used as the device under test and the gate is driven by a voltage source. At the same time, the static test Qg method is also supplemented and improved, as shown in Figure 31a.2, where (a) and (b) are the tube cut-off section measurements, in which the current source is used to drive the gate and the high-voltage source is used to drive the drain. And the tube opening section measurement, in which a high-current source is used to drive the drain, and another field effect tube or resistor is used as the current load. The measurement is divided into two sections: high voltage (HV) and high current (HC), and then fitted to form a complete Qg curve. Obviously, the JEP192 specification is clearer and more detailed.

[3] JEP192, “Guidelines for Gate Charge (QG) Test Method for SiC MOSFET” (JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, DECEMBER 2022)

The JEP192 standard provides two detailed test circuit diagrams:

- Figure 31a.1 shows the DPT circuit, a new dynamic testing method that uses a voltage source to drive the gate and specifies the lower MOSFET as the DUT.
- Figure 31a.2 illustrates the static Qg testing method, which includes:
  - (a) and (b) sections of turn-off, using a general current source to drive the gate and a high-voltage source to drive the drain.
  - Turn-on sections, where a high-current source is used to drive the drain with a MOSFET as current load or using a resistor load.

The test is divided into high-voltage (HV) and high-current (HC) two parts, two result curves are then fitted to form the complete Qg curve.

The JEP192 guidelines provide much clearer and more detailed instructions compared to the previous standard.

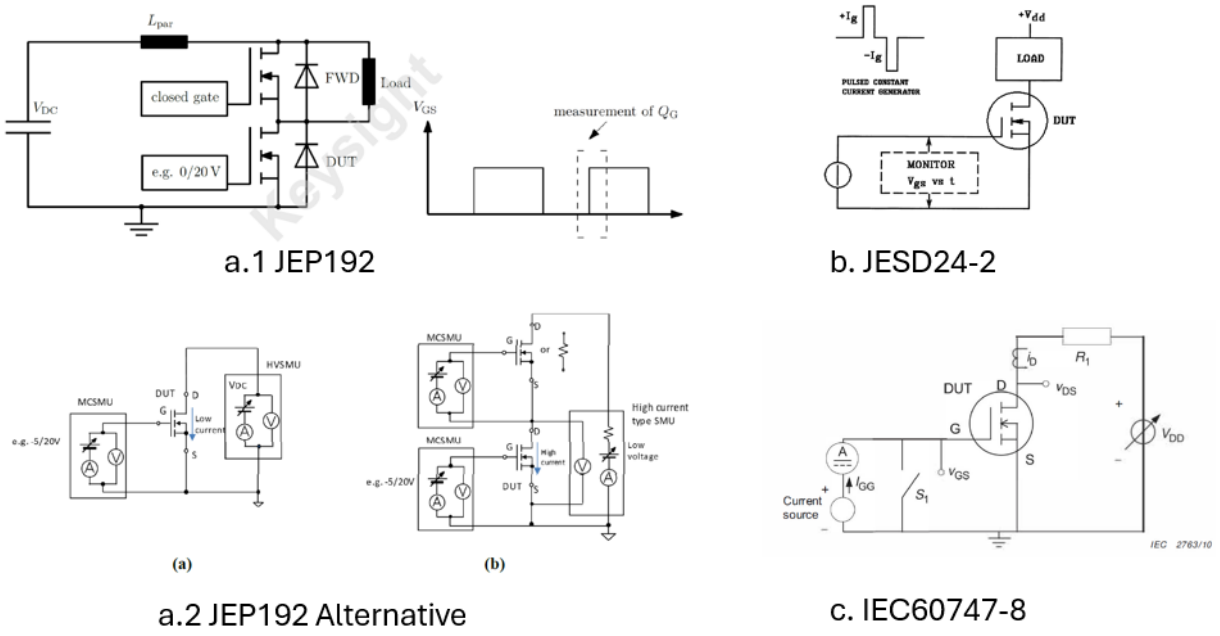


Figure 31. Schematic Diagram of The New And Old Standard

2. **The Miller plateau curve is significantly different**

Due to the typical short-channel (DIBL) effect in SiC MOSFETs, their Miller plateau exhibits a pronounced slope, unlike Si-based devices, which have a relatively flat Miller plateau, as shown in Figure 32 The Miller plateau represents the charge supplied to Cgd (gate-drain capacitance), which means that if the old expansion method is still used, Qgd would exceed the charge contribution from Cgd. Therefore, as shown in Figure 32, JEP192 defines Qgd by taking the knee point from the a-b segment as the starting point for Qgd, and then extending it horizontally. The intersection with the reverse extension of the c segment is considered the endpoint for Qgd. This ensures that the JEP192 method is downward compatible. The Qgd results measured for Si devices using JEP192 are theoretically the same as those from the JESD24-2 standard.

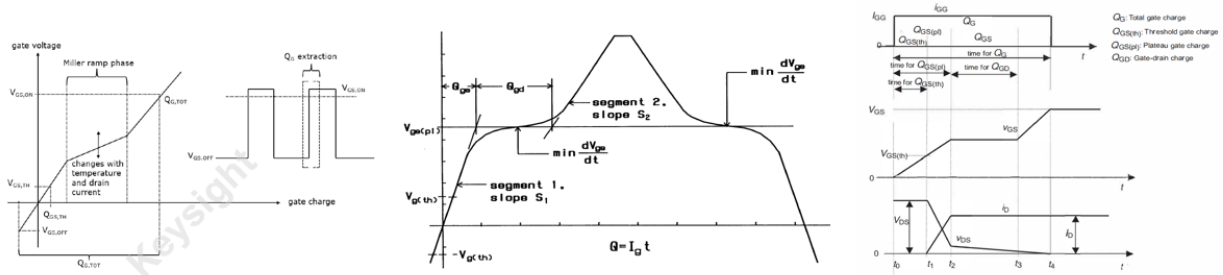


Figure 32. Defination Difference in Miller Plateau between New and Old Standards

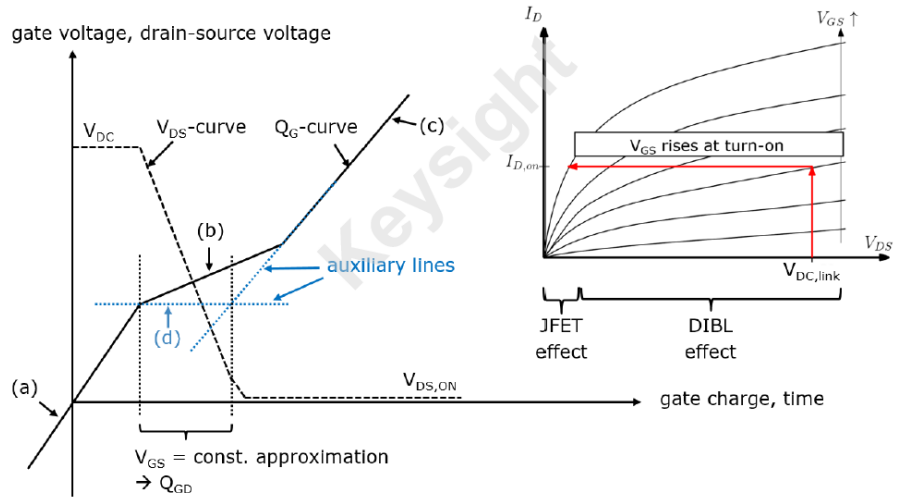


Figure 33. Qgd Expansion Method Specified in JEP192

Turn-on Qg and Turn-off Qg

SiC devices have another new characteristic due to gate-oxide interface state defects, which cause threshold voltage drift. When a certain pre-stress voltage is applied to the gate, the threshold voltage (Vgs_th) experiences drift, which is called Vgs_th hysteresis in JEP192. In theory, when measuring Qg from turn-on pulses and from turn-off pulses, the threshold voltage during the SiC device's operation is different. This leads to a higher Miller plateau during the turn-off process, as shown in Figure 34. As a result, the Qg_s_pl during the turn-on and turn-off phases will differ, but this does not affect Qgd. JEP192 addresses this issue by standardizing the calculation of Qg using the turn-on pulse.

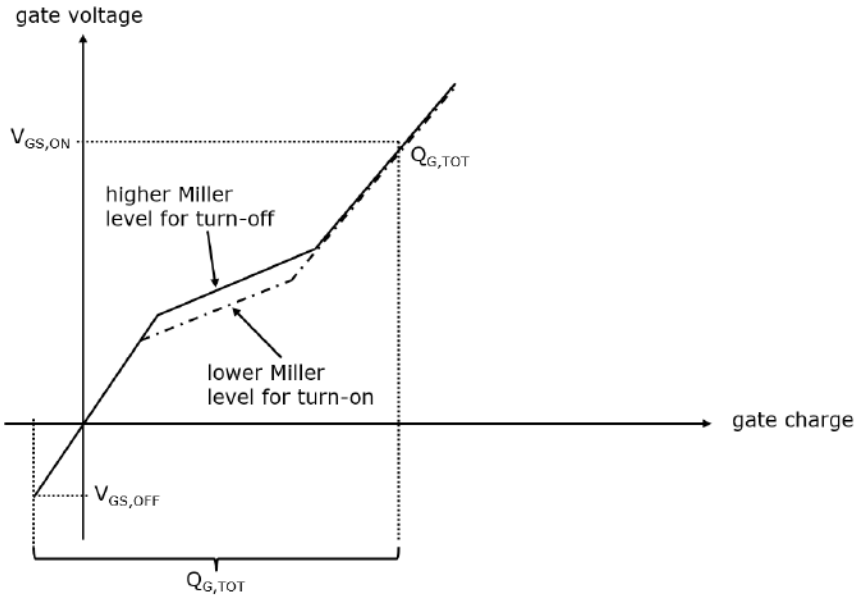


Figure 34. JEP192 Turn-On and Turn-Off Qg Difference Due to Vgs_Th Hysteresis

It can be seen that there are significant differences between the old and new standards, with the new guidelines being more detailed and specific. The JEP192 standard provides more precise methods for measuring Qg due to the hysteresis effects observed in SiC MOSFETs, leading to variations in the Qg curves between the turn-on and turn-off processes. Both Keysight's static parameter analyzer B1505A/B1506A and dynamic parameter analyzer PD1500A / PD1550A have been updated with software that supports the new JEP192 standard. Figure 35 demonstrates the expansion of the Qg curve for a specific SiC MOSFET device using the B1505A static parameter analyzer, with noticeable differences in Qgd and Vgs_pl when measured according to the two different standards.

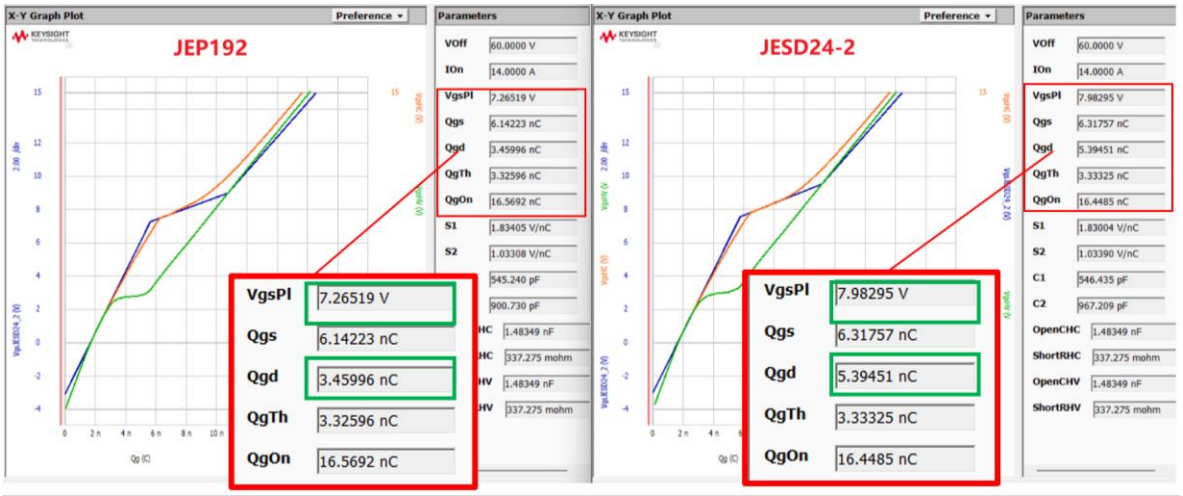


Figure 35. B1505A Test Results for The Same Sic Device Based on The Old And New Specifications

Measurement Analysis: Comparison of Two Testing Methods

Can Qg be measured both with a dynamic testing analyzer and a static parameter analyzer? Are the results comparable? This is a question many engineers might ask. Below, we will compare the results of testing the same device using both methods.

As shown in Figure 36, two SiC MOSFETs are tested using PD1500A and B1505A respectively. The results from both the dynamic and static methods are generally consistent, though there are slight differences. Specifically, the dynamic method yields a Qg_pl that is smaller than the static method's result, and the total Qg_total is also slightly smaller. Additionally, since the static method involves separately measuring two curves (high current and high voltage) and then fitting them, the resulting slope of the platform is slightly smaller than that obtained from the dynamic method.

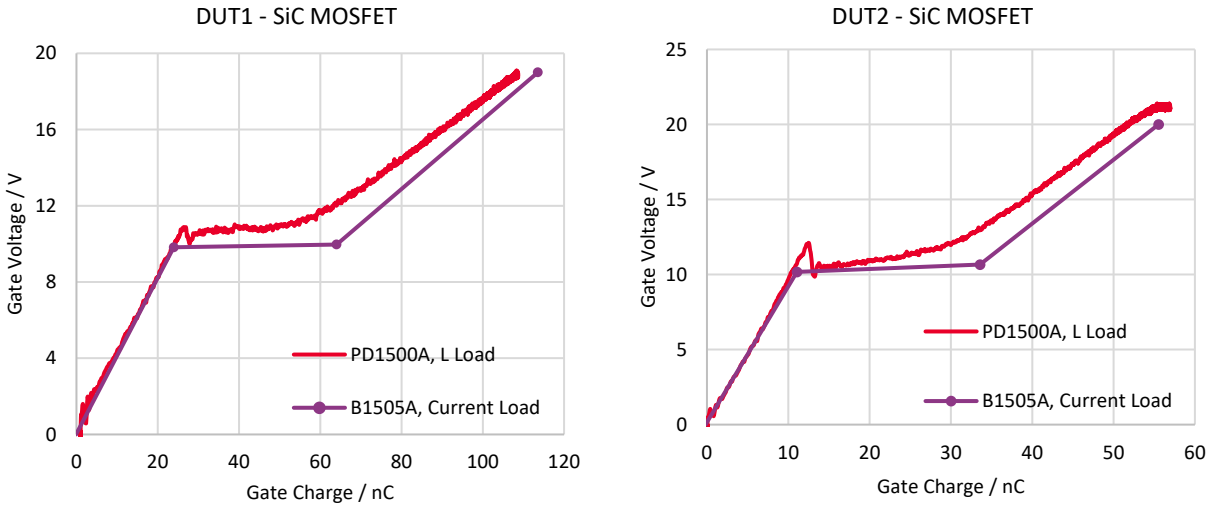


Figure 36. Comparison of static and dynamic Qg test results of SiC devices

In contrast, for a Si IGBT in the comparison test, the Qg curves obtained using both dynamic and static methods are quite similar, as shown in Figure 37.

From the above analysis, we can draw the simple conclusion that both the dynamic and static parameter analyzers can measure Qg, and their results are generally consistent. However, for testing SiC devices, it is best to specify the testing method to ensure more consistent and reliable conclusions. This helps to account for any minor differences that may arise due to the different measurement approaches.

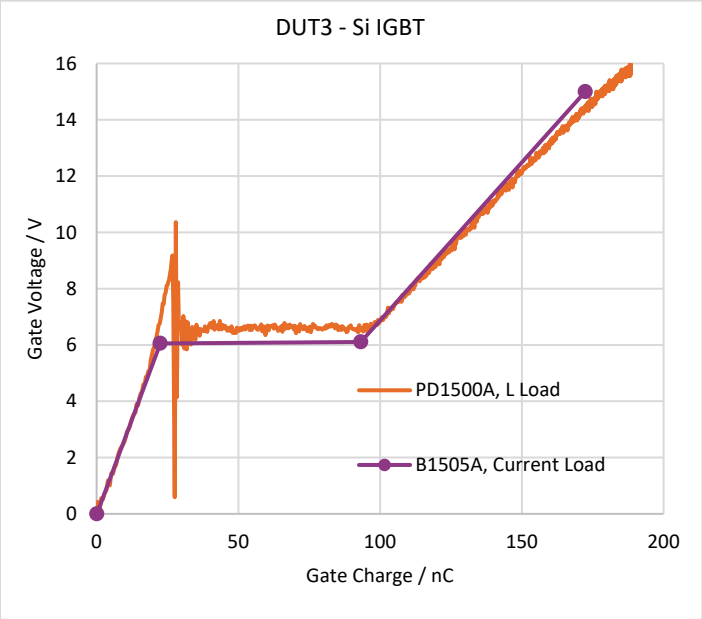


Figure 37. Comparison of static and dynamic Qg test results of Si devices

Measurement Analysis: Selection of Load Type

When measuring Qg, the choice of load can significantly affect the test results, in addition to the method used. As mentioned in previous chapters, Keysight's B1505A / B1506A static parameter analyzers can use either current loads or resistive loads for Qg testing, while Keysight's PD1500A / PD1550A dynamic parameter analyzers can use inductive loads or resistive loads.

We performed Qg tests on two devices using different loads and present the results below.

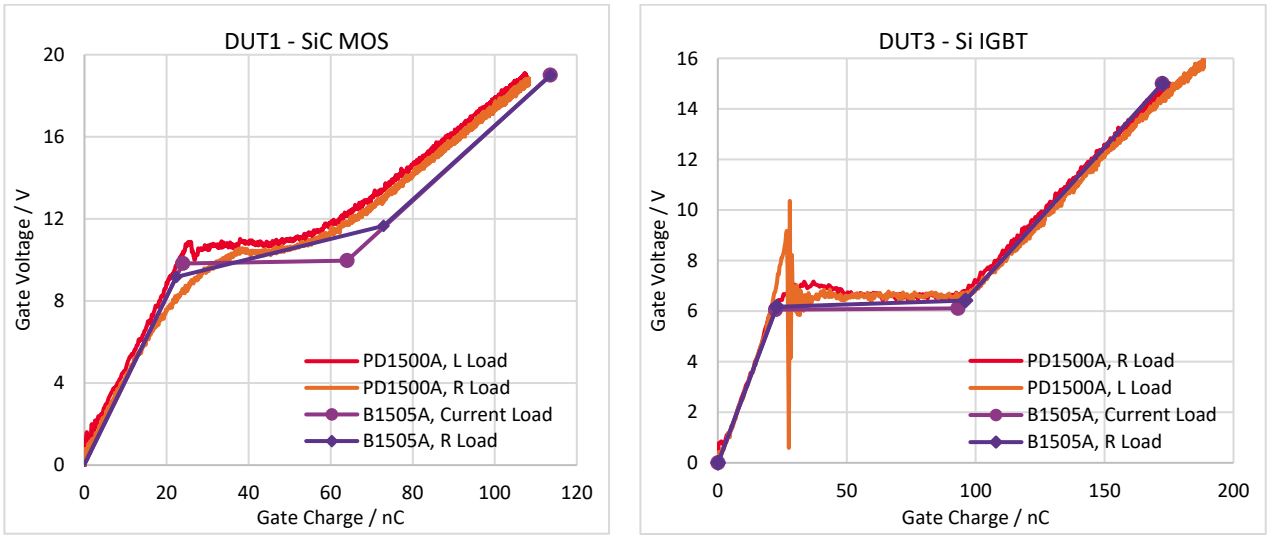


Figure 38. Comparison of different load test results

As shown in Figure 38, for SiC devices using the dynamic method, the Qg curves obtained with both resistive loads and inductive loads are generally similar. However, while the resistive load provides a smoother curve with fewer oscillations, it makes it harder to accurately identify the knee points on the curves, making it more difficult to obtain precise Qgd results. Therefore, the inductive load is preferred.

In the static method, the current load and resistive load both yield similar overall curves, but there is a difference in the slope of the Miller plateau. The resistive load results in a higher slope, while the current load gives a slightly lower slope. Compared to the resistive load, the current load is more preferred for Qg testing in the static method.

Measurement Analysis: The Impact of Hysteresis on Turn-On and Turn-Off Qg in SiC Devices

While JEP192 mentions the possibility of hysteresis effects in SiC devices during the Miller plateau portion of the turn-on and turn-off Qg curves, it does not require the measurement of turn-off Qg. For research purposes, we also conducted Qg tests for both turn-on and turn-off Qg using Keysight's DPT.

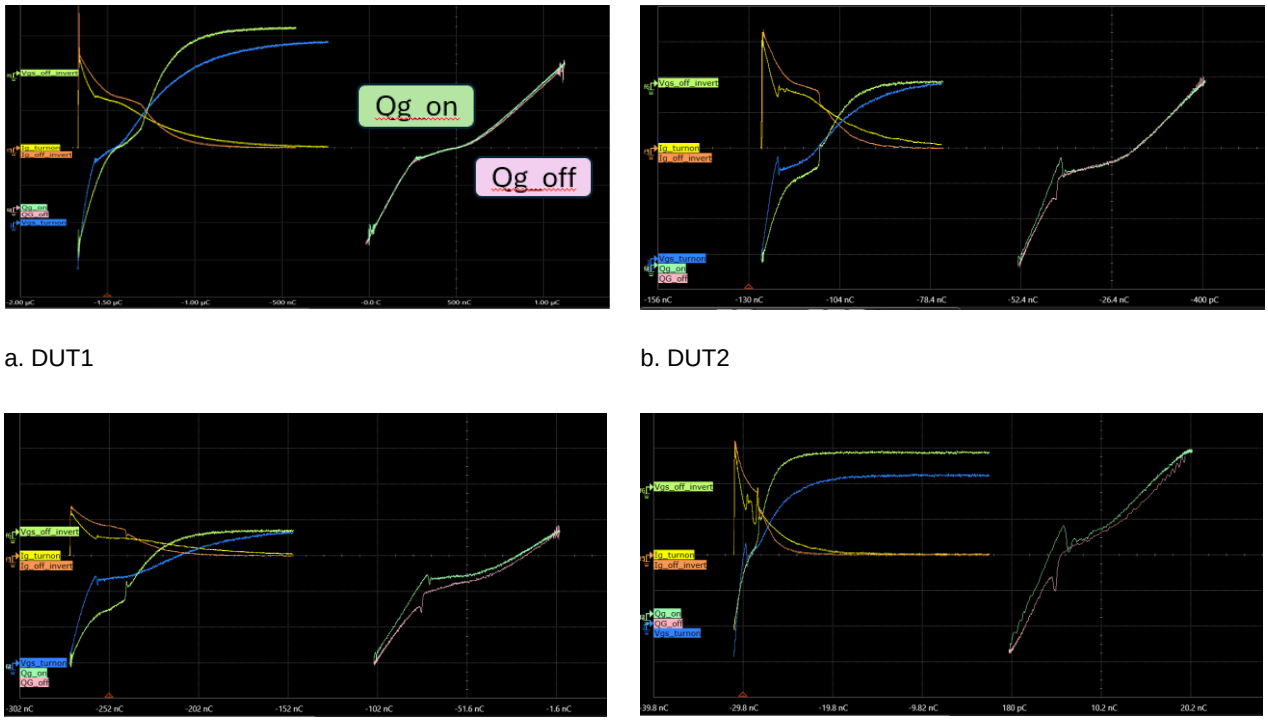
We tested four different SiC MOSFETs as shown in Figure 39 and used the oscilloscope's processing functions to obtain four sets of Qg curves. Each set of curves shows the following:

On the left side: Igs_on, Igs_off_invert, Vgs_on, and Vgs_off_invert waveforms.

On the right side: The comparison of Qg_on and Qg_off after performing an X-Y transformation.

As expected, the Igs and Vgs time-domain waveforms for turn-on and turn-off are not identical, since the processes for turning on and off are inherently different. Comparing the Qg_on and Qg_off curves, we see that the overall consistency of Qg is good, as shown in Figure 39a. Specifically, the total Qg_on_total is nearly equal to Qg_off_total. However, no noticeable hysteresis effect is observed, which differs from what JEP192 anticipates. This indicates that the threshold of the SiC device did not shift due to microsecond-level pulse stress, contrary to what was expected.

These results suggest that, for the SiC MOSFETs tested, the threshold voltage did not experience a significant drift during the turn-on and turn-off processes, which can occur in certain conditions but was not observed in this case.



a. DUT1

b. DUT2

c. DUT3

d. DUT4

Figure 39. Turn-on Qg and Turn-off Qg

Conclusion

The rapid development of the new energy sector has greatly accelerated the application of third-generation power semiconductors. Gate charge (Qg) is one of the key dynamic parameters for power semiconductor devices, directly affecting the switching time and driving losses in dynamic operating scenarios. It is a critical factor in improving the efficiency of power devices. However, due to the fast-switching speeds, small gate charge, and difficulties in controlling stray effects in third-generation semiconductors like SiC, ensuring consistency, reliability, and repeatability of gate charge measurements remains a significant challenge.

This paper addresses the unique aspects of SiC gate charge testing, introducing the two main testing methods: static and dynamic gate charge testing. It analyzes the characteristics of these methods and elaborates on the various factors influencing the accuracy of gate charge measurements. Additionally, the paper summarizes important testing considerations and measurement techniques and discusses the differences between new and old testing standards to better understand the characteristics of new devices.

Finally, through extensive comparative testing and data analysis based on Keysight's power device static and dynamic parameter test systems, we demonstrate how to more accurately and efficiently measure gate charge.

The test equipment also plays a crucial role in ensuring the accuracy and reliability of the results. All the test projects presented in this paper were conducted using Keysight's static parameter analyzers B1505A / B1506A and dynamic parameter analyzers PD1500A / PD1550A. Keysight's deep expertise in the power semiconductor industry and comprehensive understanding of measurement technology ensure the accuracy and reliability of the test data.